REMARKS

The Office Action dated November 19, 2004, has been received and carefully considered. In this response, claims 1, 2, 4-6, 8, 9-17, 21, 24, 25, 27-29, 31-33, 38, and 39 have been amended. Entry of the amendments to the claims 1, 2, 4-6, 8, 9-17, 21, 24, 25, 27-29, 31-33, 38, and 39 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE ANTICIPATION REJECTION OF CLAIMS 1, 2, 5, 6, 9, 17-21, 23, AND 33-38

On pages 2-3 of the Office Action, claims 1, 2, 5, 6, 9, 17-21, 23, and 33-38 were rejected under 35 U.S.C. § 102(b) as being anticipated by Coyle et al. (U.S. Patent No. 5,003,463). This rejection is hereby respectfully traversed with amendment.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d

1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id.

Regarding claims 1, 6, 17, and 33, the Examiner asserts that Coyle et al. discloses the present invention as claimed. Specifically, the Examiner asserts that Coyle et al. discloses a first device (18/20 and SBI 0 or MCU 22) operably coupled to a bus (SB 12), a second device (IOP 1 or MEM 0) operably coupled to the bus (SB 12), the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a first set of data to the second device (IOP 1 or MEM 0) and the second device (IOP 1 or MEM 0) transmitting a second portion of the first set of data to the first device (18/20 and SBI 0 or MCU 22) simultaneously during a first exchange slot position; and a third device (IOP 2 or MEM 1) operably coupled to the bus (SB 12), the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a second set of data to the third device (SBI 2 or MEM 1) and the third device (SBI 2 or MEM 1) transmitting a second portion of

the second set of data to the first device (18/20 and SBI 0 or MCU 22) simultaneously during a second exchange slot.

However, it is respectfully submitted that Coyle et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of: selecting a first memory device and a second memory device from among a plurality of memory devices coupled to a common bus line to exchange a first set of data; scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line, as presently recited in claim 1.

It is also respectfully submitted that Coyle et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a system for providing simultaneous bidirectional signaling in a bus topology comprising: a first memory device coupled to a bus line; a second memory device coupled to the bus line, the first memory

device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and a third memory device coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first memory device simultaneously during a second exchange slot, as presently recited in claim 6.

It is further respectfully submitted that Coyle et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory system comprising: a memory controller; a bus line coupled to the memory controller; a first memory device coupled to the bus line, the first memory device configured to simultaneously send first read data to the memory controller via the bus line and receive first write data from the memory controller via the bus line; and a second memory device coupled to the bus line, the second memory device configured to simultaneously send second read data to the memory controller via the bus line and receive

second write data from the memory controller via the bus line, as presently recited in claim 17.

It is still further respectfully submitted that Coyle et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of: during a first exchange slot, simultaneously communicating over a common bus line first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory controller; and during a second exchange slot, simultaneously communicating over the common bus line second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller, as presently recited in claim 33.

Claims 2 and 5 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2 and 5 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken

either alone or in combination, as Applicant has previously discussed.

Claim 9 is dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claim 9 should also be allowable at least by virtue of its dependency on independent claim 6. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 18-21 and 23 are dependent upon independent claim 17. Thus, since independent claim 17 should be allowable as discussed above, claims 18-21 and 23 should also be allowable at least by virtue of their dependency on independent claim 17. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 34-38 are dependent upon independent claim 33. Thus, since independent claim 33 should be allowable as discussed above, claims 34-38 should also be allowable at least by virtue of their dependency on independent claim 33. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references

taken either alone or in combination, as Applicant has previously discussed.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 5, 6, 9, 17-21, 23, and 33-38 be withdrawn.

II. THE ANTICIPATION REJECTION OF CLAIMS 1-14 AND 17-39

On pages 3-6 of the Office Action, claims 1-14 and 17-39 were rejected under 35 U.S.C. § 102(e) as being anticipated by Garlepp et al. (U.S. Patent No. 6,687,780). This rejection is hereby respectfully traversed with amendment.

Regarding claims 1, 6, 10, 17, 24, 28, 33, and 39, the Examiner asserts that Garlepp et al. discloses the present invention as claimed. Specifically, the Examiner asserts that Garlepp et al. discloses a system providing simultaneous bidirectional signaling using a bus topology comprising: a first device (256) operably coupled to a bus (252, 254); a second device (262-1) operably coupled to the bus, the first device (256) transmitting a first portion of a first set of data to the second device (262-1) and the second device (262-1) transmitting a second portion of the first set of data to the first device (256) simultaneously during a first exchange slot; and a third device (262-2) operably coupled to the bus, the first device

(256) transmitting a first portion of a second set of data to the third device (262-2) and the third device (262-2) transmitting a second portion of the second set of data to the first device (256) simultaneously during a second exchange slot.

However, it is respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of: selecting a first memory device and a second memory device from among a plurality of memory devices coupled to a common bus line to exchange a first set of data; scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line, as presently recited in claim 1.

It is also respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a system for providing simultaneous bidirectional signaling in a bus topology

comprising: a first memory device coupled to a bus line; a second memory device coupled to the bus line, the first memory device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and a third memory device coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first memory device simultaneously during a second exchange slot, as presently recited in claim 6.

It is further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory device coupled to a bus line in a bus topology for providing simultaneous bidirectional signaling comprising: a transmitter circuit configured to provide additive signaling, the transmitter circuit applying transmit signals to the bus line; a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus line,

the transmitter circuit and the receiver circuit operating during an exchange slot, as presently recited in claim 10.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory system comprising: a memory controller; a bus line coupled to the memory controller; a first memory device coupled to the bus line, the first memory device configured to simultaneously send first read data to the memory controller via the bus line and receive first write data from the memory controller via the bus line; and a second memory device coupled to the bus line, the second memory device configured to simultaneously send second read data to the memory controller via the bus line and receive second write data from the memory controller via the bus line, as presently recited in claim 17.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory device comprising: a transmitter circuit configured to drive a bus line with read data during an exchange slot while write data is present on the bus line; a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to receive the write data from the bus line during the exchange

slot while the transmitter circuit is driving the bus line with the read data; and a memory circuit operably coupled to the transmitter circuit and the receiver circuit, the memory circuit configured to provide the read data and to store the write data, as presently recited in claim 24.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory controller comprising: a transmitter circuit configured to drive a bus line with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device is present on the bus line; a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to receive the first read data from the bus line during the first exchange slot while the transmitter circuit is driving the bus line with the first write data, as presently recited in claim 28.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of: during a first exchange slot, simultaneously

communicating over a common bus line first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory controller; and during a second exchange slot, simultaneously communicating over the common bus line second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller, as presently recited in claim 33.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a system for bidirectional communication of data over a common bus line comprising: a first device operably coupled to the common bus line, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit buffer to hold first-to-third data; a second device operably coupled to the common bus line, the second device comprising a second-to-first transmit buffer to hold second-to-first data; a third device operably coupled to the common bus line, the third device comprising a third-to-first transmit buffer to hold third-to-first data; and a scheduler operably coupled to the common bus line, the scheduler scheduling the

first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus line simultaneously during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-first data over the common bus line simultaneously during a second exchange slot, the scheduler introducing a turnaround delay sufficient to prevent inter-symbol interferences between the first exchange slot and the second exchange slot, as presently recited in claim 39.

Claims 2-5 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-5 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 7-9 are dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claims 7-9 should also be allowable at least by virtue of their dependency on independent claim 6. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 11-14 are dependent upon independent claim 10. Thus, since independent claim 10 should be allowable as discussed above, claims 11-14 should also be allowable at least by virtue of their dependency on independent claim 10. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 18-23 are dependent upon independent claim 17. Thus, since independent claim 17 should be allowable as discussed above, claims 18-23 should also be allowable at least by virtue of their dependency on independent claim 17. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 25-27 are dependent upon independent claim 24. Thus, since independent claim 24 should be allowable as discussed above, claims 25-27 should also be allowable at least by virtue of their dependency on independent claim 24. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references

taken either alone or in combination, as Applicant has previously discussed.

Claims 29-32 are dependent upon independent claim 28. Thus, since independent claim 28 should be allowable as discussed above, claims 29-32 should also be allowable at least by virtue of their dependency on independent claim 28. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 34-38 are dependent upon independent claim 33. Thus, since independent claim 33 should be allowable as discussed above, claims 34-38 should also be allowable at least by virtue of their dependency on independent claim 33. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

At this point it should be noted that (1) the present application and Garlepp et al. have a common inventor, Frederick A. Ware, and (2) the present application and Garlepp et al. are commonly owned. Thus, Applicant reserves the right to swear behind the filing date of Garlepp et al. under a 37 C.F.R. §

1.131 Declaration. While Applicant retains the right to perform this action, it is believed that Garlepp et al. fails to disclose the claimed invention as discussed above.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-14 and 17-39 be withdrawn.

III. THE ANTICIPATION REJECTION OF CLAIMS 1, 2, 6, AND 9-16

On pages 6-8 of the Office Action, claims 1, 2, 6, and 9-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Borkar et al. (U.S. Patent No. 5,604,450). This rejection is hereby respectfully traversed with amendment.

Regarding claims 1, 2, 6, and 9-16, the Examiner asserts that Borkar et al. discloses the present invention as claimed. Specifically, the Examiner asserts that Borkar et al. discloses a system providing simultaneous bidirectional signaling using a bus topology comprising: a first device (Core A) operably coupled to a bus (21); a second device (Core B) operably coupled to the bus (21), the first device (Core A) transmitting a first portion of a first set of data to the second device (Core B) and the second device (262-1) transmitting a second portion of the first set of data to the first device (256) simultaneously during a first exchange slot; and a third device ("additional"

components?) operably coupled to the bus (21), the first device (Core A) transmitting a first portion of a second set of data to the third device ("additional" components?) and the third device ("additional" components?) transmitting a second portion of the second set of data to the first device (Core A) simultaneously during a second exchange slot.

However, it is respectfully submitted that Borkar et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of: selecting a first memory device and a second memory device from among a plurality of memory devices coupled to a common bus line to exchange a first set of data; scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line, as presently recited in claim 1.

It is also respectfully submitted that Borkar et al. fails to disclose, or even suggest, either alone or in combination

with the other cited references, a system for providing simultaneous bidirectional signaling in a bus topology comprising: a first memory device coupled to a bus line; a second memory device coupled to the bus line, the first memory device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and a third memory device coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first memory device simultaneously during a second exchange slot, as presently recited in claim 6.

It is further respectfully submitted that Borkar et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory device coupled to a bus line in a bus topology for providing simultaneous bidirectional signaling comprising: a transmitter circuit configured to provide additive signaling, the transmitter circuit applying transmit signals to the bus line; a receiver circuit operably coupled to the transmitter circuit,

the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus line, the transmitter circuit and the receiver circuit operating during an exchange slot, as presently recited in claim 10.

Claim 2 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 2 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claim 9 are dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claim 9 should also be allowable at least by virtue of its dependency on independent claim 6. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 11-16 are dependent upon independent claim 10. Thus, since independent claim 10 should be allowable as discussed above, claims 11-16 should also be allowable at least by virtue of their dependency on independent claim 10. Moreover, these claims recite additional features which are not

claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 6, and 9-16 be withdrawn.

IV. THE ANTICIPATION REJECTION OF CLAIMS 1, 2, 6, AND 9-16

On pages 8-10 of the Office Action, claims 1, 2, 6, and 9-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ishibashi et al. (U.S. Patent No. 5,872,471). This rejection is hereby respectfully traversed with amendment.

Regarding claims 1, 2, 6, and 9-16, the Examiner asserts that Ishibashi et al. discloses the present invention as claimed. Specifically, the Examiner asserts that Ishibashi et al. discloses a system providing simultaneous bidirectional signaling using a bus topology comprising: a first device (1A) operably coupled to a bus (3); a second device (1B) operably coupled to the bus (3), the first device (1A) transmitting a first portion of a first set of data to the second device (1B) and the second device (1B) transmitting a second portion of the first set of data to the first device (1A) simultaneously during a first exchange slot; and a third device ("additional" LSI?)

operably coupled to the bus (3), the first device (1A) transmitting a first portion of a second set of data to the third device ("additional" LSI?) and the third device ("additional" LSI?) transmitting a second portion of the second set of data to the first device (1A) simultaneously during a second exchange slot.

However, it is respectfully submitted that Ishibashi et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of: selecting a first memory device and a second memory device from among a plurality of memory devices coupled to a common bus line to exchange a first set of data; scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line, as presently recited in claim 1.

It is also respectfully submitted that Ishibashi et al. fails to disclose, or even suggest, either alone or in

combination with the other cited references, a system for providing simultaneous bidirectional signaling in a bus topology comprising: a first memory device coupled to a bus line; a second memory device coupled to the bus line, the first memory device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and a third memory device coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first memory device simultaneously during a second exchange slot, as presently recited in claim 6.

It is further respectfully submitted that Ishibashi et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory device coupled to a bus line in a bus topology for providing simultaneous bidirectional signaling comprising: a transmitter circuit configured to provide additive signaling, the transmitter circuit applying transmit signals to the bus line; a receiver circuit operably coupled to the transmitter circuit,

the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus line, the transmitter circuit and the receiver circuit operating during an exchange slot, as presently recited in claim 10.

Claim 2 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 2 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claim 9 are dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claim 9 should also be allowable at least by virtue of its dependency on independent claim 6. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 11-16 are dependent upon independent claim 10. Thus, since independent claim 10 should be allowable as discussed above, claims 11-16 should also be allowable at least by virtue of their dependency on independent claim 10. Moreover, these claims recite additional features which are not

claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 6, and 9-16 be withdrawn.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 6, and 9-16 be withdrawn.

V. THE OBVIOUSNESS REJECTION OF CLAIMS 3, 4, 7, 8, AND 22

On page 10 of the Office Action, claims 3, 4, 7, 8, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Coyle et al. (U.S. Patent No. 5,003,463). This rejections is hereby respectfully traversed.

As stated in MPEP § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Also, as stated in MPEP § 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Further, as stated in MPEP § 2143.03, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). Additionally, as stated in MPEP § 2141.02, a prior art reference must be considered in its

entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Finally, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Regarding claims 3, 4, 7, 8, and 22, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide Coyle et al. with "turn around delay" between time slows, since the Examiner takes Official Notice that using a turn around delay between time slots are old and well known for preventing data interference; and using such a "turn around delay" in Coyle et al. involves only routine skill in the art.

Claims 3 and 4 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 3 and 4 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 7 and 8 are dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claims 7 and 8 should also be allowable at least by virtue of their dependency on independent claim 6. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claim 22 is dependent upon independent claim 17. Thus, since independent claim 17 should be allowable as discussed above, claim 22 should also be allowable at least by virtue of its dependency on independent claim 17. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 3, 4, 7, 8, and 22 be withdrawn.

VI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The

Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

TEA/vrp

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

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